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PTO/SB/05 (08/00)
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1 53(b))

Attorney Docket No.	**061606-1241**
First Named Inventor	**Chapman**
Title	**Apparatus and Method to Allow a Frame Check Sequence to Determine the Updating of Adaptive Receiver Parameters of a High Speed Communication Device**
Express Mail Label No.	**EL492180196US**

APPLICATION ELEMENTS

See MPEP Chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

1. [X] Fee Transmittal Form *(e.g., PTO/SB/17)* *(Submit an original, and a duplicate for fee processing)*
2. [ ] Applicant claims small entity status
3. [X] Specification *[Total Pages 27]* *(preferred arrangement set forth below)*
   - Descriptive title of the invention
   - Cross References to Related Applications
   - Statement Regarding Fed Sponsored R&D
   - Reference to sequence listing, a table, or a computer program listing appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
4. [X] Drawing(s) *(35 USC 113)* *[Total Sheets 7]*
5. Oath or Declaration *[Total Pages 2]*
   - a. [ ] Newly Executed (original or copy)
   - b. [X] Copy from a prior application (37 CFR §1 63(d)) *(for continuation/divisional with Box 17 completed)*
   - i [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR §1.63(d)(2) and 1.33(b)
6. [ ] Application Data Sheet See 37 CFR 1 76
7. [ ] CD-ROM or CD-R in duplicate, large table or Computer Program (Appendix)
8. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   - a. [ ] Computer Readable Copy (CRF)
   - b. Specification Sequence Listing on:
     - i. [ ] CD-ROM or CD-R (2 copies), or
     - ii. [ ] Paper
   - c. [ ] Statements verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

9. [ ] Assignment Papers (cover sheet & Documents(s))
10. [ ] 37 CFR 3.73(b) Statement *(when there is an assignee)* [X] Power of Attorney
11. [ ] English Translation Document *(if applicable)*
12. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
13. [X] Preliminary Amendment
14. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [ ] Other:

17. If a CONTINUING APPLICATION, *check appropriate box and supply the requisite information below and in a preliminary amendment, or in an Application Data Sheet under 37 CFR 1.76:*

☒ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No: **09**/021,850

Prior application information: ***Examiner*** *Pham, B.* ***Group / Art Unit:*** *2731*

For CONTINUATION OR DIVISIONAL APPS only the entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference This incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts

18. CORRESPONDENCE ADDRESS

☒ *Customer Number or Bar Code Label* **24504** *(Insert Customer No. or Attach bar code label here)* *or* ☐ *Correspondence address below*

NAME	**Scott A. Horstemeyer** **Thomas, Kayden, Horstemeyer & Risley, L.L.P.**				
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CITY	**Atlanta**	*STATE*	**Georgia**	*ZIP CODE*	**30339-5948**
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Name (Prnt/Type)	**Michael J. Tempel**	*Registration No (Attorney/Agent)*	**41,344**
Signature	Michael J. Tempel	*Date*	11/20/00

Burden Hour Statement: This form is estimated to take 0 2 hours to complete Time will vary depending upon the needs of the individual case Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office Washington, DC 20231 DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS SEND TO Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

JC806 U.S. PTO 11/20/00

JC598 U.S. PTO 09/716787 11/20/00

PTO/SB/17 (1/98)
Approved for use through 09/30/2001 OMB 0651-0032
Patent and Trademark Office: U S DEPARTMENT OF COMMERCE

FEE TRANSMITTAL for FY 2000

Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT | ($) 984.00

Complete If Known	
Application Number	To Be Assigned
Filing Date	Even Date Herewith
First Named Inventor	Chapman
Examiner Name	To Be Assigned
Group / Art Unit	To Be Assigned
Attorney Docket No.	061606-1241

METHOD OF PAYMENT

1. ☒ The Commissioner is hereby authorized to charge to the following Deposit Account,

Deposit Account Number: 16-0255

Deposit Account Name: Paradyne Corporation's

☐ Charge all indicated fees and any additional fee required or credit any overpayment.

☒ Charge any additional fee required and requested to credit any overpayment.

☐ Applicant claims small entity status. See 37 CFR 1 27

2. ☐ **Payment Enclosed:**

☐ Check ☐ Money Order ☐ Credit Card

FEE CALCULATION

1. BASIC FILING FEE

Large Fee Code	Entity Fee ($)	Small Fee Code	Entity Fee ($)	Fee Description	Fee Paid
101	710	201	355	Utility filing fee	$710
106	320	206	160	Design filing fee	$
107	490	207	245	Plant filing fee	$
108	710	208	355	Reissue filing fee	$
114	150	214	75	Provisional filing fee	$

SUBTOTAL (1) ($) 710

2. EXTRA CLAIM FEES

			Extra Claims		Fee from below		Fee Paid
Total Claims	33	-20**=	13	x	18.00	=	234
Independent Claims	3	-3** =	0	x	80.00	=	0
Multiple Dependent					270.00	=	

**or number previously paid, if greater; For Reissue, see below

Large Fee Code	Entity Fee ($)	Small Fee Code	Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	80	202	40	Independent Claims in excess of 3
104	270	204	135	Multiple dependent claims in excess of 3
109	80	209	40	**Reissue independent claims over original patent
110	18	210	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)944

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Fee Code	Entity Fee ($)	Small Fee Code	Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	390	216	195	Extension of time within second month	
117	890	217	445	Extension of time within third month	
118	1,390	218	695	Extension of time within fourth month	
128	1,890	228	945	Extension of time within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a pubic use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,240	241	620	Petition to revive - unintentional	
142	1,240	242	620	Utility issue fee (or reissue)	
143	440	243	220	Design issue fee	
144	600	244	300	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt.	
581	40	581	40	Recording each patent assignment per property (time number of properties)	40.00
146	710	246	355	Filing a submission after final rejection (37 CFR 1.129(a))	
149	710	249	355	For each additional invention to be examined (37 CFR 1.129(b))	
179	710	279	355	Request for Continued Examination (RCE)	
169	900	169	9000	Request for expedited examination of a design application	
				Other fee (specify) _____	
				Other fee (specify) _____	

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) 40

SUBMITTED BY			Complete (if applicable)
Typed or Printed Name	Michael J. Tempel		Reg Number 41,344
Signature		Date 11/20/00	Deposit Account User ID

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Chapman

Serial No.: 09/021,850

Group No.: 2731

Examiner: Pham, B.

Filed: February 11, 1998

For: **Apparatus and Method to Allow a Frame Check Sequence to Determine the Updating of Adaptive Receiver Parameters of a High Speed Communication Device**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

NOTIFICATION OF FILING OF CONTINUING APPLICATION

Notification is hereby being made of the filing of a:

☒ Continuation

☐ Continuation-in-part

application for this case

☒ concurrently herewith

☐ on _____

Michael J. Tempel; Reg. No. 41,344

Tel. No.: (770) 933-9500

THOMAS, KAYDEN,
HORSTEMEYER & RISLEY, L.L.P.
100 Galleria Parkway, Suite 1750
Atlanta, GA 30339

CERTIFICATE OF MAILING (37 CFR 1.8)

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited on the date shown below with the United States Postal Service in an envelope addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231.

(check and complete appropriate item below):

37 CFR 1.8(a)

☒ with sufficient postage as first class mail

or

CFR 1.10

☐ as "Express Mail Post Office to Addressee" Mailing Label No. _____

Date: November 20, 2000

Gloria L. Knox

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on November 20, 2000

Gloria L. Knox

In re application of: Chapman

Serial Number: To Be Assigned

Filing Date: Even Date Herewith

Group No.: To Be Assigned

Examiner: To Be Assigned

Title: **Apparatus and Method to Allow a Frame Check Sequence to Determine the Updating of Adaptive Receiver Parameters of a High Speed Communication Device**

Attached are the following documents for filing with the USPTO:

Fee Transmittal Page
U.S. Continuation Application - Consisting of:
  22 Pages of Specification
  4 Pages of Claims
  1 Page of Abstract
Formal Drawings (7 Pages)
Utility Application Transmittal
Authorization to Charge Deposit Account 16-0255 the amount of $984.00 to cover application filing fees
Declaration and Power of Attorney (Copy)
Notification of Filing of Continuing Application (Copy)
Preliminary Amendment
Postcard

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:	)	
	)	
Chapman	)	Examiner: To Be Assigned
	)	
Serial No.: To Be Assigned	)	Art Unit: To Be Assigned
	)	
Filed: (Herewith)	)	Docket No.: 061606-1241
	)	
For: Apparatus and Method to Allow a Frame Check Sequence to Determine the Updating of Adaptive Receiver Parameters of a High Speed Communication Device	)	

PRELIMINARY AMENDMENT

Honorable Commissioner
of Patents and Trademarks
Washington, DC 20231

Sir:

Applicant submits the following preliminary amendment and remarks.

It is not believed that extensions of time or fees for net addition of claims are required, beyond those which may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. §1.136(a), and any fee required therefor (including fees for net addition of claims) are hereby authorized to be charged to Paradyne Corporation's Deposit Account No. 16-0255.

I hereby certify that this correspondence is being deposited with the United States Postal Service, "**Express Mail Post Office to Addressee**" service under 37 CFR §1.10 on the date indicated below: The envelope has been given U.S. Postal Service Express Mail Post Office To Assistant Commissioner for Patents, Washington, D.C. 20231"
Package # EL492180196US

Date: November 20, 2000

Signature – Gloria L. Knox

Prior to Examination, please amend the above-identified application as follows:

AMENDMENTS

In the Specification

Amend the specification as follows:

Page 1, line 6 delete "This application" and substitute therefor --This application is a continuation of application Serial No. 09/021,850, filed February 11, 1998, which--.

Page 3, line 21 delete "equalizers" and substitute therefor -- equalizer's --.

Page 4, line 16 after "Therefore" insert -- , --.

Page 4, line 24 after "parameters" insert -- , --.

Page 8, line 10 after "Fig. 2" insert -- ; and --.

Page 9, line 2 after "but not limited to," insert -- the invention can be used to update --.

Page 10, line 15 after "200" insert -- , --.

Page 13, line 7 delete "non linear" and substitute therefor -- nonlinear --.

Page 13, line 8 delete "884" and substitute therefor -- 84 --.

Page 13, line 17 after "emphasis" insert -- filter --.

Page 13, lines 22 and 23 delete "non linear" and substitute therefor -- nonlinear --.

Page 14, line 4 after "emphasis" insert -- filter --.

Page 14, line 7 delete "preemphasis" and substitute therefor -- pre emphasis --.

Page 15, line 3 delete "preemphasis" and substitute therefor -- pre emphasis --.

Page 15, line 3 after "preemphasis" insert -- filter --.

Page 15, line 6 delete "preemphasis" and substitute therefor -- pre emphasis --.

Page 15, line 10 delete "preemphasis" and substitute therefor -- pre emphasis --.

Page 15, line 10 after "preemphasis" insert -- filter --.

Page 15, line 11 delete "preemphasis" and substitute therefor -- pre emphasis --.

Page 18, line 21 after "190," insert -- which --.

In The Claims

In accordance with 37 C.F.R. § 1.121, please amend the following claims by inserting the language that is underlined ("__") and deleting the language that is enclosed in brackets ("[ ]").

1. (Amended) A digital subscriber line (DSL) communication device, comprising:

a receiver for developing a received signal; and

a digital signal processor (DSP) configured to perform layer two error detection in the receiver by computing a frame check sequence (FCS) on each frame of said received signal.

10. (Amended) A method for updating adaptive parameters in a digital subscriber line (DSL) communication device, comprising the steps of:

developing, in a receiver, a received signal; and

performing, in a digital signal processor (DSP) located in the receiver, layer two error detection by computing a frame check sequence (FCS) on each frame of said received signal.

19. (Amended) A computer readable medium having a program for updating adaptive parameters in a digital subscriber line (DSL) communication device, the program comprising:

means for developing[, in a receiver,] a received signal in a receiver; and

means for performing, in a digital signal processor (DSP) located in the receiver, layer two error detection by computing a frame check sequence (FCS) on each frame of said received signal.

Please add the following new claims:

28. (Newly Added) The apparatus as defined in claim 2, wherein said frame check sequence is used to calculate the adaptive parameters of a device chosen from the group consisting of an equalizer, an echo-canceller, an adaptive gain device, and a timing loop.

29. (Newly Added) The apparatus as defined in claim 2, wherein said frame check sequence is used to adapt a receive margin level based on said received signal.

30. (Newly Added) The method as defined in claim 11, further comprising the step of using said frame check sequence to calculate the adaptive parameters of a device chosen from the group consisting of an equalizer, an echo-canceller, an adaptive gain device, a and timing loop.

31. (Newly Added) The method as defined in claim 11, wherein said frame check sequence is used to adapt a receive margin level based on said received signal.

32. (Newly Added) The program as defined in claim 20, wherein said frame check sequence is used to calculate the adaptive parameters of a device chosen from the group consisting of an equalizer, an echo-canceller, an adaptive gain device, and a timing loop.

33. (Newly Added) The program as defined in claim 20, wherein said frame check sequence is used to adapt a receive margin level based on said received signal.

CONCLUSION

Applicants respectfully submit that the presently pending claims are in condition for allowance. If the Examiner intends to take further action by means other that a notice of allowability, then the Examiner is respectfully requested to contact the undersigned attorney if he so desires or if he believes it to be necessary.

Respectfully Submitted,

Michael J. Tempel
Registration No. 41,344

Thomas, Kayden, Horstemeyer & Risley
100 Galleria Parkway, N.W.
Suite 1750
Atlanta, Georgia 30339-5948
(770) 933-9500

Patent Application

TKHR Ref. No.61606-1241

TO ALL WHOM IT MAY CONCERN

Be it known that I, Joseph Quinn Chapman, residing at 9040 Baywood Park Drive, Seminole, Florida 33777, a citizen of the United States of America, have invented certain new and useful improvements in an

APPARATUS AND METHOD TO ALLOW A FRAME CHECK SEQUENCE TO DETERMINE THE UPDATING OF ADAPTIVE RECEIVER PARAMETERS OF A HIGH SPEED COMMUNICATION DEVICE

of which the following is a specification.

EXPRESS MAIL

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Express Mail No. EL492180196US

Signature Nova L Knox

APPARATUS AND METHOD TO ALLOW A FRAME CHECK SEQUENCE TO DETERMINE THE UPDATING OF ADAPTIVE RECEIVER PARAMETERS OF A HIGH SPEED COMMUNICATION DEVICE

CROSS REFERENCE TO RELATED APPLICATION

This application claims priority to and the benefit of the filing date of co-pending and commonly assigned provisional application entitled **THE FRAME CHECK SEQUENCE DETERMINES UPDATING A HIGH-SPEED MULTIPOINT MODEM'S EQUALIZER COEFFICIENTS,** assigned serial number 60/036,006, and filed March 5, 1997, incorporated herein by reference.

FIELD OF THE INVENTION

The present invention relates generally to data communications, and more particularly, to a method and apparatus to determine the updating of a high speed communication device's adaptive receiver parameters.

BACKGROUND OF THE INVENTION

The field of data communications typically uses modems, or communication devices, to convey information from one location to another. Digital Subscriber Line (DSL) technology now enables communications devices to communicate large amounts of data. This communication scheme adheres generally to a model, known as the Open Systems Interconnect (OSI) Seven-Layer model. This model specifies the parameters and conditions under which information is formatted and transferred over a given communications network. A general background of the OSI seven layer model follows.

In 1978, a framework of international standards for computer network architecture known as OSI (Open Systems Interconnect) was developed. The OSI reference model of network architecture consists of seven layers. From the lowest to

the highest, the layers are: (1) the physical layer; (2) the datalink layer; (3) the network layer; (4) the transport layer; (5) the session layer; (6) the presentation layer; and (7) the application layer. Each layer uses the layer below it to provide a service to the layer above it. The lower layers are implemented by lower level protocols which define the electrical and physical standards, perform the byte ordering of the data, and govern the transmission and error detection and correction of the bit stream. The higher layers are implemented by higher level protocols which deal with, *inter alia*, data formatting, terminal-to-computer dialogue, character sets, and sequencing of messages.

Layer 1, the physical layer, controls the direct host-to-host communication between the hardware of the end users' data terminal equipment (*e.g.*, a modem connected to a PC).

Layer 2, the datalink layer, generally fragments the data to prepare it to be sent on the physical layer, receives acknowledgment frames, performs error checking, and re-transmits frames which have been incorrectly received.

Layer 3, the network layer, generally controls the routing of packets of data from the sender to the receiver via the datalink layer, and it is used by the transport layer. An example of the network layer is Internet Protocol (IP) which is the network layer for the TCP/IP protocol widely used on Ethernet networks. In contrast to the OSI seven-layer architecture, TCP/IP (Transmission Control Protocol over Internet Protocol) is a five-layer architecture which generally consists of the network layer and the transport layer protocols.

Layer 4, the transport layer, determines how the network layer should be used to provide a point-to-point, virtual, error-free connection so that the end point devices send and receive uncorrupted messages in the correct order. This layer establishes and dissolves connections between hosts. It is used by the session layer. TCP is an example of the transport layer.

Layer 5, the session layer, uses the transport layer and is used by the presentation layer. The session layer establishes a connection between processes on different hosts. It handles the creation of sessions between hosts as well as security issues.

Layer 6, the presentation layer, attempts to minimize the noticeability of differences between hosts and performs functions such as text compression and format and code conversion.

Layer 7, the application layer, is used by the presentation layer to provide the user with a localized representation of data which is independent of the format used on the network. The application layer is concerned with the user's view of the network and generally deals with resource allocation, network transparency and problem partitioning.

Existing digital subscriber line (DSL) devices operating in the full-duplex mode conduct equalizer training and coefficient determination using previously stored channel operating parameters determined by operations performed in the datalink layer (layer 2). For example, U.S. Patent No. 4,621,366 discloses a modem that acquires, stores and reinitializes the modem equalizer using channel operating parameters determined during an initial training sequence. For a subsequent transmission, the modem uses the stored coefficients and parameters during a shortened training sequence. While this operation takes place in layer one of the OSI seven layer model, the aforementioned modem only uses the equalizers mean-square-error vector to determine the probability of erroneous equalizer updating. Various channel conditions may cause the modem's equalizer to track inappropriately. By using only the modem's mean square error vector to determine the probability of erroneous equalizer updating, existing modems fail to take advantage of the layer two framing and frame check sequence available to a device's digital signal processor (DSP) in layer one of the OSI seven layer model.

In a multipoint communication environment including a control device and a

plurality of remote devices, each device includes a transmitter and a receiver. Each device uses messages incorporating a protocol which includes the receiving device's address and a poll bit. The poll bit is set by the control device to indicate an expected response from a particular remote device. During an initial start up sequence, reception of a relatively long training sequence is necessary before data communication can proceed. The receiver parameters, including adaptive equalizer coefficients, for each remote device that has successfully completed the aforementioned lengthy training sequence are stored in a memory located within the control device. The control device will store the parameters for each remote device in a memory location dedicated to that particular remote device.

During subsequent transmissions, a relatively short training sequence, which synchronizes the control device receiver, and identifies the transmitting remote device is used. During the reception of the subsequent message, parameters within the control device's equalizer, and other adaptive devices parameters, are adaptive and are modified to compensate for any changes in the channel characteristics.

Therefore, it would be desirable to provide a more robust technique for updating adaptive receiver parameters by allowing a DSP in a control device to use the layer two error detection results to decide whether the new adaptive parameters, available during the shortened training period, should be saved and used or discarded in favor of the last known good parameters.

SUMMARY OF THE INVENTION

In a communications channel using a DSL device, a standard training period is used to establish communication line parameters which enable the devices to negotiate a clear communication path. Once the initial training period is complete, for example, once the devices have established a successful connection, the control device will periodically poll the remote devices in a half-duplex operating mode to determine

whether any remote device has any information to send to the control device. Should the remote device have information to transmit, a shortened training period takes place.

During this shortened training period, the remote devices will transmit signals and the then current communication line parameters will be calculated by the control device, which enables the receiver in the control device to update various adaptive parameters including equalizer, adaptive gain control, timing loop, echo-canceler, and cross talk canceler parameters. During this shortened training period a frame check sequence is executed by the digital signal processor located in the control device. The results of the frame check sequence executed by the DSP in the control device will determine the quality of the newly calculated parameters.

While the foregoing is applicable to various adaptive receiver parameters, the following discussion will be with respect to the updating of a communication device's adaptive equalizer coefficients. It should be noted that the concepts of the present invention are applicable to other adaptive receiver parameters.

If the frame check sequence is error free, the receiver of the control device will update its adaptive parameters based upon the most recently calculated parameters. If the frame check sequence indicates an error in the transmission, the receiver of the control device will discard the newly calculated parameters and will instead load the last known good channel parameters into its adaptive devices and proceed with transmission. During this shortened training period the DSP uses the layer two error detection results to determine whether or not to save the new parameters. Optionally, the DSP may also use the mean-squared-error vector of the equalizer as additional input in determining whether or not to save the newly calculated parameters. This arrangement allows the DSP access to a more precise and robust channel parameter measurement in order to determine whether the user data contains errors prior to updating the adaptive equalizer coefficients. If this latest data contains errors, the device will not update the adaptive parameters, but will instead use the last known good

parameters. If this latest data is error free, *i.e.*, within the range of acceptable errors, the device will use this data to update the adaptive parameters.

The apparatus and method to allow a frame check sequence to determine the updating of adaptive receiver parameters of a high speed communication device can be embodied in a digital subscriber line (DSL) communication device, comprising a receiver for developing a received signal and a digital signal processor (DSP) configured to perform layer two error detection by computing a frame check sequence (FCS) on each frame of the received signal. The present invention also includes means for saving the adaptive parameters of an adaptive device located within the receiver of a control device, the adaptive parameters calculated by the DSP, if the frame check sequence indicates that the received signal is error free.

The present invention further includes means for using existing adaptive parameters of an adaptive device located within the receiver of the control device if the frame check sequence indicates that the received signal contains errors. This essentially allows the DSP to perform layer two framing and the frame check sequence in layer one, the physical layer, heretofore never performed by a DSP within a communication device.

The present invention can also be conceptualized as a method for re-establishing a connection in a digital subscriber line (DSL) communication device, comprising the steps of developing a received signal in a receiver and performing, in a digital signal processor (DSP), layer two error detection by computing a frame check sequence (FCS) on each frame of the received signal. The method also includes the step of saving the adaptive parameters of an adaptive device located within the receiver, the adaptive parameters calculated by the DSP, if the frame check sequence indicates that the received signal is error free. If the frame check sequence indicates that the received signal contains errors, the device uses existing parameters for all adaptive devices located within the receiver.

The invention has numerous advantages, a few of which are delineated hereafter, as merely examples.

An advantage of the present invention is that it allows a communication device (or a DSP in a communication device) to perform OSI layer two frame check sequencing and error correction. This results in an increased level of error detection because the DSP now has access to the layer two error correction framing information in addition to the mean-square-error vector of the equalizer.

Another advantage of the present invention is that it provides a more robust, better performing technique for updating the adaptive receiver parameters.

Another advantage of the present invention is that it allows the equalizer filter taps to adjust gracefully to changing line conditions.

Another advantage of the present invention is that it allows for error correction in an uncoded modulation environment.

Another advantage of the present invention is that it is simple in design, reliable in operation, and its design lends itself to economical mass production in DSL devices.

Other objects, features, and advantages of the present invention will become apparent to one with skill in the art upon examination of the following drawings and detailed description. It is intended that all such additional objects, features, and advantages be included herein within the scope of the present invention, as defined in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention, as defined in the claims, can be better understood with reference to the following drawings. The drawings are not necessarily to scale, emphasis instead being placed on clearly illustrating the principles of the present invention.

Fig. 1 is a schematic view illustrating a multipoint communications environment in which communication devices including the frame check sequence and adaptive parameter update logic operate;

Fig. 2 is a block diagram of a communications device including the frame check sequence and adaptive parameter update logic of the present invention;

Fig. 3 is a schematic view illustrating a transmitter of the communication device of Fig. 2;

Figs. 4A and 4B collectively illustrate a schematic view of the receiver of the communication device of Fig. 2;

Fig. 5 is a schematic view illustrating the layer two framing and frame check sequence performed by the frame check sequence and adaptive parameter update logic of Fig. 2

Fig. 6 is a flow chart illustrating the operation of the frame check sequence and adaptive parameter update logic of the communication device of Fig. 2.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The apparatus and method to allow a frame check sequence to determine the updating of adaptive receiver parameters of a high speed communication device can be implemented in software, hardware, or a combination thereof. In the preferred embodiment, the elements of the present invention are implemented in software that is stored in a memory and that configures and drives a suitable digital signal processor (DSP) situated in a communication device. However, the foregoing software can be stored on any computer-readable medium for transport or for use by or in connection with any suitable computer-related system or method. In the context of this document, a computer-readable medium is an electronic, magnetic, optical, or other physical device or means that can contain or store a computer program for use by or in connection with a computer-related system or method. Furthermore, the present invention is applicable to all modulation schemes as known in the art, and while discussed in the preferred embodiment as useful for updating the adaptive coefficients

of an adaptive equalizer, the present invention is useful for updating any adaptive receiver parameter. For example, but not limited to, adaptive gain control, timing loop, echo-canceler, and cross talk canceler parameters.

Fig. 1, shows a schematic view illustrating a multipoint communications environment 11 in which communication devices employing the frame check sequence and adaptive parameter update logic of the present invention operate. Remote location 16 is connected to central office location 12 via communication channel 14. In the preferred embodiment, control device 13 and remote device 18 are illustratively digital subscriber line (DSL) communication devices. However, the concepts of the present invention are applicable to various other types of communication devices employing adaptive parameters.

Located at central office location 12 is control device 13. Communication channel 14 is typically the copper wire pair that extends between a telephone company central office and a remote residential, business, or any other location served by local telephone service. Remote location 16 may contain a plurality of remote devices 18 connecting a plurality of user devices 17 to communication channel 14 via communication bus 19. Communication bus 19 is illustratively the copper wiring infrastructure used throughout a remote location to connect remote devices 18 to communication channel 14. Remote devices 18 are typically located in a residential or business location.

Furthermore, all of the functionality described herein occurs in layer 1, the physical layer, of the OSI seven layer model, *i.e.*, is performed by the communication device or a DSP within a communication device.

Architecture

Now referring to Fig. 2, shown is a schematic view illustrating control device 13 of Fig. 1 including the frame check sequence and adaptive parameter update logic

200 of the present invention. Typically, control device 13 will transmit signals to remote devices 18 over communications channel 14. Similarly remote devices 18 will transmit signals to control device 13.

Control device 13 contains frame check sequence (FCS) and adaptive parameter update logic 200 which enables the control device to perform a frame check sequence in the digital signal processor (OSI layer one) using information available in the data link layer (OSI layer two) to determine whether to update adaptive parameters using newly calculated channel parameters, or whether to discard the new parameters and use last known good saved parameters.

Still referring to Fig. 2, control device 13 contains conventional components as is known in the art of data communications. Digital Signal Processor (DSP) 21 controls the operation of, and includes, control device's transmitter 22 and receiver 23, and couples to line interface 26 to gain access to communications channel 14. Also included in DSP 21 of control device 13 is FCS and adaptive parameter update logic 200, which enables control device 18 to more reliably and robustly perform error detection. Also contained within control device 13 is memory 27, which also includes FCS and adaptive parameter update logic 200. In a preferred embodiment, the logic of the present invention is executed within DSP 21 and is therefore shown as residing in both memory 27 and in DSP 21. While depicted as discrete components, control device 13 may illustratively be contained within DSP 21, *i.e.*, DSP 21 can perform all the functionality of control device 13.

Prior to discussing the present invention, the general operation of a communication device employing the FCS and adaptive parameter update logic 200 of the present invention will be discussed. While the preferred embodiment is discussed with respect to circular signal space constellations and carrierless amplitude/phase (CAP) modulation, the concepts of the present invention are applicable to all modulation schemes and all signal space constellation configurations.

With reference to Fig. 3, shown is a preferred embodiment of a transmitter 22 of modem 13 employing the FCS and adaptive parameter update logic 200 of the present invention. Illustratively, an ISA bus, a standard computer bus which eliminates the need for interfaces, supplies data, in the form of a data word that can be either 16 or 32 bits for the preferred embodiment, on line 31 to tx buffer 32. Tx buffer 32 outputs a signal representative of information to be transmitted on line 34. The information signal, or N bit word on line 34 includes the setting of a poll bit, which indicates to each remote device that a communication is starting. The use of the poll bit will be described herein in detail with reference to Figs. 4A, 5 and 6. The N bit word on line 34 next has its frame check sequence (FCS) calculated 190 in DSP 21 and in accordance with the present invention.

Optionally, the N bit word is next input on line 41 to scrambler 42. Scrambler 42 can be either a self synchronized scrambler or a preset free running scrambler as is known in the art. Depending on the application, the preset scrambler may have some advantage, as in the case of using Reed-Solomon coding. If scrambler 42 is employed, a scrambled N bit word is output on line 44. The scrambled N bit word is then sent on line 44 to register 46. This data word is transformed into an N bit word by counting bits and shifting to arrive at a smaller number of bits, in this example, an N bit data word is segmented into N-2 most significant bits (msb's) and 2 least significant bits (lsb's). By employing a circular signal space constellation, N can be any number.

Optionally, in order to allow the transmission of fractional bit rates as is known in the art of data communications, register 46 can include a modulus converter or other means such as constellation switching or shell mapping. Modulus conversion is a well known technique in the art of communications for allowing the transmission of fractional bit rates, and is described in U.S. Patent No. 5,103,227. Constellation switching allows the transmission of fractional bit rates by, for example, first transmitting 6 bits in one symbol and 7 bits in the next symbol if it is desired to

transmit 6 ½ bits. For 6 ¾ bits one would transmit 7 bits per symbol for three symbol cycles and transmit 6 bits per symbol for the fourth symbol cycle. Shell mapping blocks the data into frames and a shell mapping algorithm, such as that described in the V.34 specification, is used to map the frames of data into a constellation of a certain size.

The resulting N-2 bit word on line 47 is supplied to mapper 54 which maps the N-2 bit word, in this preferred embodiment, into a multidimensional circular signal space constellation, resulting in mapped N-2 msb's, represented by a 2-dimensional vector, supplied on line 56 to rotator 57. Other signal space constellations may be used while employing the concepts of the present invention.

Next, the 2 lsb's on line 48 are operated upon by phase encoder 67. Phase encoder 67 is designed to develop a rotation vector 68 using the 2 lsb's supplied by the register. This rotation vector is output on line 69 and combined in rotator 57 with the mapped N-2 bit word on line 56 to form a phase rotated signal, thus creating a symmetric circular signal space constellation. Optionally, phase encoder 67 includes differential phase encoder 62 which encodes the 2 lsb's of the N bit word to develop 2 differential bits. These 2 differential bits are output on line 59 and combined with the 2 lsb's from register 46 in adder 61 and become part of the rotation vector 68.

Rotator 57 performs vector multiplication on the rotation vector on line 69 and the mapped N-2 msb's on line 56 to cause a phase rotation, thus producing the final quadrant symmetric circular signal space constellation on line 58.

The circular constellation on line 58 is then supplied to precoder 72. Precoder 72 comprises a finite impulse response (FIR) filter 77 in feedback loop 79. While a FIR filter is illustrated, any filter can be employed. FIR filter 77 is followed by modulo operation 78. Modulo operation 78 operates on the signal on line 76 whereby if the voltage of the signal on line 76 is greater than a preset value, twice that value is subtracted from the signal until the signal is less than or equal to the preset value. Or,

if a value more negative than a negative preset value, twice that value is added to the signal until the signal is greater than or equal to the negative preset value. The modulo modified signal is then supplied to subtractor 71 where it is subtracted from the signal on line 58 for input to FIR filter 77. After processing by precoder 72 the circular constellation is supplied on line 74 to scaler 81.

Scaler 81 multiplies the circular constellation by a scale function of the data rate and supplies a complex number comprising X and Y values on line 82 to non linear encoder 884. The scale function allows a single table to be used to implement the mapper at all data rates. Nonlinear encoder 84 encodes the signal as described in commonly assigned U.S. Patent No. 5,265,127 to Betts et al. titled "NON-LINEAR ENCODER AND DECODER FOR INFORMATION TRANSMISSION THROUGH NON-LINEAR CHANNELS" dated November 23, 1993.

The encoded signal output from non linear encoder 84 is next supplied through baud timing switch 85 to TX Hilbert filter 86. Baud switch 85 is controlled by train encoder function 51 via line 52. TX Hilbert filter 86 operates on the signal to provide a carrierless amplitude/phase modulation (CAP) modulated signal on line 87 to transmit pre emphasis 88. Alternatively, the scaled circular constellation supplied through switch 85 can be modulated using modulator 92, using a technique such as discrete multitone modulation (DMT), or coded or uncoded quadrature amplitude modulation (QAM). Modulator 92 provides the sine and cosine components of a carrier frequency, or the X and Y values of the carrier frequency as is known in the art, on line 94 to multiplier 96. Multiplier 96 combines the X and Y components with the output of non linear encoder 84 for input to TX Hilbert filter 86 which provides a bandpass output at a certain frequency range. The concepts and features of the present invention as claimed can be practiced using various modulation schemes, such as CAP modulation, DMT modulation, or a coded or uncoded modulation technique such as QAM or PAM. All modulation schemes are contemplated by the present invention.

The operation of the communications system disclosed thus far, *i.e.*, up to TX Hilbert filter 86, occurs at the symbol rate of the modem, with the symbol rate equal to the bandwidth of the modem, thus allowing the use of reduced cost components. The output of TX Hilbert filter 86, transmit pre emphasis 88 and DAC 91 are computed at the sample rate, which is typically three times that of the symbol rate.

The modulated signal on line 87 is supplied to transmit pre emphasis filter 88. As is known in the art, transmit pre emphasis filter 88 adds preemphasis to the signal, and is typically an FIR filter as is known in the art. The pre emphasized transmit signal is next supplied on line 89 to digital to analog converter 91 for conversion to an analog signal that can be transmitted conventionally over communication channel 14 as is known in the art. Optionally, pre emphasis filter 88 can reside after the DAC to provide pre emphasis in the analog domain.

Now referring to Fig. 4A, shown is a schematic view of the receiver section 23 of the communication device of Fig. 2.

The received signal is input from communication channel 14 on line 101 to analog to digital converter 102 for conversion to the digital domain as known in the art. The digital received signal is supplied through baud timing switch 106 to RX Hilbert filter 114. The filtered signal is output from RX Hilbert filter 114 on line 119. In the case of QAM modulation, demodulator 116 provides the sine and cosine components of the carrier frequency on line 117 to multiplier 118 for combination with the output of RX Hilbert filter 114. Furthermore, other demodulation techniques, such as DMT or PAM, can be used. The demodulated output is provided on line 119 to adaptive gain control (AGC) circuit 121. AGC circuit 121 multiplies the demodulated received signal by gain factor 122. The AGC compensated signal is then supplied on line 124 to equalizer 126. Equalizer 126 is a known in the art finite impulse response (FIR) filter with adaptive parameters, the adaptive parameters being updated in accordance with the

FCS and adaptive parameter update logic 200 of the present invention to be discussed hereafter.

Optionally, receive preemphasis 107 may be employed to further enhance the communication signal. This is particularly advantageous when an echo canceler is used where a replica of the transmit echo is subtracted from the input to the RX Hilbert filter 114 at the output of the receive preemphasis filter 107.

Baud timing switch 106 and baud timing switch 85 of Fig. 3 are controlled by a timing signal supplied on line 104 from voltage controlled crystal oscillator (VCXO) 108. VCXO 108 receives its input signal on line 109 from baud timing device 111, which operates on the received signal output from receive preemphasis 107, if employed, and from ADC 102 if receive preemphasis is omitted. Baud timing device 111 develops a timing signal used to drive VCXO 108, which in turn drives baud timing switches 106 and 85.

The coefficients of equalizer 126 are adaptively updated by subtracting the input of scaler 134 from the ideal reference signal output of slicer 138, which is upscaled by scaler 139 and output on line 141. The output of subtractor 142 is the error signal that is supplied via line 144 to register 148. Register 148 contains the last known good equalizer working coefficients calculated by DSP 21 based upon the message sent by remote device 18 to control device 13, and supplies these working coefficients to equalizer 126 via line 153 during the time that control device 13 is polling remote device 18. Specifically, control device 13 recalls the last known good equalizer coefficients each time it sends a query to remote device 18.

When remote device 18 responds to the poll, the signal from remote device 18 contains new channel parameters. In accordance with the present invention, at this time, FCS and adaptive parameter update logic 200 located in DSP 21 and illustrated as block diagram components 146 and 148 of Fig. 4A, and components 190 and 196 of Fig. 4B, calculates the frame check sequence (to be discussed in detail with respect to

Fig. 5) in order to determine whether the most recently received signal contains errors. If the transmission from remote device 18 is error free, the most recently calculated coefficients 146 sent on line 152 are saved and used to update equalizer 126 via line 151. These coefficients will be recalled by control device 13 the next time a transmission takes place. If the most recently received signal contains an error, as determined by the FCS and adaptive parameter update logic 200, the most recently calculated channel parameters in register 146 are discarded in favor of the last known good parameters in register 148.

Control device 13 will continue to use the last known good coefficients from register 148 until the next transmission from a remote device 18, where the FCS and adaptive parameter update logic 200 will again perform the error calculation to determine whether to update equalizer 126 with the latest channel parameters from register 146.

The equalized signal is supplied through baud timing switch 127 to nonlinear decoder 128 which performs the inverse operation of nonlinear encoder 84. The output of nonlinear decoder 128 is supplied on line 129 to noise whitening filter 131. Noise whitening filter 131 is a part of the receiver precoder and includes a FIR filter and an adder. Noise whitening filter 131 performs the inverse operation of precoder 82 in order to provide the correct channel response to scaler 134. The output of noise whitening filter 131 is supplied on line 132 to scaler 134 which operates on the received signal with a 1/scale factor. The 1/scale factor is a function of the data rate depending on the number of points in the constellation. The output of scaler 134 is the normalized X and Y components representing the values of the symbols in the circular signal space constellation.

The normalized output of scaler 134 is supplied to slicer 138, which performs the inverse operation of mapper 54. Slicer 138 generates the nearest ideal reference

vector X_R, Y_R to the received X, Y vector. Because the signal is normalized, one slicer can be used for all data rates.

The input of scaler 134 is also supplied to subtractor 142 along with the upscaled output of slicer 138 through scaler 139. Scaler 139 upscales the output of slicer 138 for input to subtractor 142. Adder 142 subtracts the input to the 1/scale factor from the upscaled output of slicer 138 to obtain an error signal on line 144 to update FIR filter tap coefficients of equalizer 126. Improved precision is achieved using the input of scaler 138 and the upscaled references on line 141.

The output of slicer 138 is then supplied on line 149 to precoder reconstruction filter 152. Precoder reconstruction filter 152 removes the modulo operation applied in transmitter 22 of Fig. 3. The output of slicer 138 represents ideal reference signals of the X and Y values of the signal space constellation. These ideal values are input to subtractor 151, which subtracts the output of FIR filter 157. The output of subtractor 151 is fed into FIR filter 157 and adder 158. The output of FIR filter 157 feeds subtractor 151 and modulo operation 159. Modulo operation 159 is then added to the input to FIR filter 157 by adder 158 resulting in the removal of the modulo operation applied in transmitter 22 of Fig. 3.

With reference now to Fig. 4B, phase decoder 168 decodes the 2 lsb's of the received signal by analyzing the output of precoder reconstruction filter 152 to determine which phase rotation was transmitted.

Phase slicer 164 slices the circular signal space constellation to separate the 2 lsb's for input on line 166 to derotation vector operator 167. Derotation vector operator 167 outputs a derotation vector on line 176 which is combined with the output of precoder reconstruction filter 152 on line 161 in rotator 177. Rotator 177 multiplies the X and Y values from precoder reconstruction filter 152 with the derotation vector from phase decoder 168 for input to slicer 179 on line 178. As in the transmitter,

phase decoder 168 optionally includes differential decoder 169 to decode the 2 lsb's if they were differentially encoded in the transmitter.

Differential decoder 169 develops 2 differential bits on line 171 in order to recover the 2 lsb's of the N bit word. The 2 differential bits are subtracted in subtractor 172 from the output of phase slicer 164 on line 173 and input on line 174 to optional descrambler 182.

Differential decoder 169 eliminates the need for a trellis decoder, thus reducing processor cycles. In the absence of differential decoder 169, the 2 lsb's are passed through subtractor 172 on line 173 with nothing subtracted from them, essentially passing them directly to optional descrambler 182.

Slicer 179 converts the complex vector X, Y into the original N-2 msb's. Slicer 179 performs a mathematical operation in that it masks each axis to slice the axis. Slicer 179 then multiplies one of the axes of the constellation by a scale factor, and then adds the other masked axis value to the result. The output of slicer 179 is the N-2 msb data that was originally transmitted which is then combined with the decoded 2 least significant bits from phase decoder 168 to form the decoded N bit word.

If included, optional scrambler 182 descrambles the n bit word and supplies the word to register 186, which performs the inverse operation of register 46 in transmitter 22. The output of register 186 is supplied on line 187 to RX buffer 188, which in turn supplies the data word to frame check sequence and header test logic 190. FCS and header test logic 190, is part of the frame check sequence and adaptive parameter update logic 200, performs the layer two error detection in the DSP on a per message basis by calculating the FCS on a per frame basis. The result of the FCS is used as an indication of whether or not to save the updated equalizer adaptive coefficients. If the FCS indicates an error free transmission, the updated coefficients are provided on line 152 to register 146 (Fig. 4A) and used to update the adaptive coefficients of equalizer

126. The data word is then supplied on line 192 to error counter 194, which provides a running error count.

Referring now to Fig. 5, shown is a schematic view illustrating the layer two framing and frame check sequence 190 performed by the frame check sequence and adaptive parameter update logic 200 of Fig. 2.

Message frame 190 includes multiple fields that represent the layer two framing and frame check sequence operation occurring within the DSP 21 of Fig. 2, which has heretofore only occurred in OSI layer two as part of the data link protocol. By moving this framing and FCS calculation into the DSP (OSI layer 1) the DSP can use the layer two error detection results to more robustly determine whether to update adaptive parameters. Optionally, the mean squared error vector of the equalizer may also be used to provide additional accuracy in determining whether the recently received signal contains errors.

The protocol incorporates a High-Level Data Link Control (HDLC) type protocol. Field 201 contains the destination address field of the polled remote device. Field 202 contains the source address field. Field 204 contains the control byte. Field 204 encodes three types of frames. Information frames that carry user data, supervisory frames that carry physical layer messages, and management frames that carry management messages. Field 204 also encodes polling, flow control, and address management functions.

Field 206 contains the byte count header. Field 206 contains the number of bytes that are in the frame following the header. This count allows the DSP to know in advance when the frame being received is to end.

Field 207 contains the frame check sequence header, field 208 contains the message information, and field 209 contains the frame check sequence information.

Field 208 contains the payload. Frame 209 carries the user data. In management frames the information field carries management data or messages. In supervisory frames, the information field caries physical layer messages.

Operation

Referring now to Fig. 6, shown is an operational flow chart 200 of the frame check sequence and adaptive parameter update logic 200 of the present invention.

The operation of the present invention occurs after a standard training procedure has been completed and the control device 13 and remote devices 18 have been transmitting and receiving data in normal operating mode. This procedure includes the control device training its adaptive devices, including its equalizer using coefficients calculated by the DSP, on channel parameters determined when messages are received from remote device 18.

The following description of the operation of the frame check sequence and adaptive parameter update logic 200 assumes that both control device 13 and remote devices 18 have previously established a communication link, gone silent, and wish to reestablish the communication link. Furthermore, while the following illustrates a single remote device communicating with a control device, the principles of the present invention contemplate a control device communicating with a plurality of remote devices on the communication channel.

In block 211 the control device transmits a message having the poll bit set to a remote device. Having the poll bit set alerts the remote device that the control device is inquiring whether the remote device has any information to transmit to the control device. In block 212 the control device, knowing which remote device is being polled, recalls the equalizer coefficients, and any other adaptive parameters for that particular remote device, and loads the coefficients into a working active receiver area (register 148 of Fig. 4A).

In block 214 the remote device receives the message having the poll bit set from the control device and, if it has any information to transmit, responds with a message.

In block 217 the message from the remote device is received by the control device. The control device receives the message and calculates the frame check sequence as described with respect to Figs. 4B and 5. Simultaneously, the control device 13 is calculating new adaptive coefficients based upon this newly received message. The FCS calculation is performed by the DSP in the control device using the layer two error detection results, and optionally, in conjunction with the mean squared error vector, to determine whether to save the most recently calculated adaptive coefficients.

In block 218, the DSP in the control modem decides whether or not to save the latest channel parameters. If the frame check calculation performed in the DSP indicates that the latest transmission is error free, block 219 indicates that the control device will save the most recently calculated coefficients to a memory location, register 148 of Fig. 4A associated with the particular remote device that complete the transmission, and continue the transmission session using the latest adaptive coefficients.

If the frame check calculation performed by the DSP indicates errors in the most recent transmission, block 221 indicates that the control device will discard the most recently received coefficients and will use the last known good coefficients, register 146 of Fig. 4A, for the particular remote device.

It will be obvious to those skilled in the art that many modifications and variations may be made to the preferred embodiments of the present invention, as set forth above, without departing substantially from the principles of the present invention. For example, but not limited to the following, it is possible to implement the present invention to update adaptive coefficients of an echo canceler, adaptive gain control, and timing loop updates. All such modifications and variations are intended to be included herein within the scope of the present invention, as defined in the claims that follow.

CLAIMS

Therefore, the following is claimed:

1. A digital subscriber line (DSL) communication device, comprising:

a receiver for developing a received signal; and

a digital signal processor (DSP) configured to perform layer two error detection by computing a frame check sequence (FCS) on each frame of said received signal.

2. The apparatus as defined in claim 1, further comprising means for saving the adaptive parameters of an adaptive device located within said receiver, and calculated by said DSP, if said frame check sequence indicates that said received signal is error free.

3. The apparatus as defined in claim 1, further comprising means for using existing parameters of an adaptive device located within said receiver if said frame check sequence indicates that said received signal contains errors.

4. The apparatus as defined in claim 1, wherein said DSL device operates in a multipoint environment.

5. The apparatus as defined in claim 1, wherein said DSL device operates in a half duplex environment.

6. The apparatus as defined in claim 1, wherein said DSL device operates in a full duplex environment.

7. The apparatus as defined in claim 1, wherein said DSL device operates in an asymmetrical duplex environment.

8. The apparatus as defined in claim 1, wherein said layer two error detection resides in layer one of the OSI seven layer model.

9. The apparatus as defined in claim 2, wherein said means for saving the adaptive parameters of an adaptive device located within said receiver resides in layer one of the OSI seven layer model.

10. A method for updating adaptive parameters in a digital subscriber line (DSL) communication device, comprising the steps of:

developing, in a receiver, a received signal; and

performing, in a digital signal processor (DSP), layer two error detection by computing a frame check sequence (FCS) on each frame of said received signal.

11. The method as defined in claim 10, further comprising the step of saving the adaptive parameters of an adaptive device located within said receiver and calculated by said DSP if said frame check sequence indicates that said received signal is error free.

12. The method as defined in claim 10, further comprising the step of using existing parameters of an adaptive device located within said receiver if said frame check sequence indicates that said received signal contains errors.

13. The method as defined in claim 10, wherein said DSL device operates in a multipoint environment.

14. The method as defined in claim 10, wherein said DSL device operates in a half duplex environment.

15. The method as defined in claim 10, wherein said DSL device operates in a full duplex environment.

16. The method as defined in claim 10, wherein said DSL device operates in an asymmetrical duplex environment.

17. The method as defined in claim 10, wherein said step of performing layer two error detection occurs in layer one of the OSI seven layer model.

18. The method as defined in claim 11, wherein said step of saving the adaptive parameters of an adaptive device located within said receiver occurs in layer one of the OSI seven layer model.

19. A computer readable medium having a program for updating adaptive parameters in a digital subscriber line (DSL) communication device, the program comprising:

means for developing, in a receiver, a received signal; and

means for performing, in a digital signal processor (DSP), layer two error detection by computing a frame check sequence (FCS) on each frame of said received signal.

20. The program as defined in claim 19, further comprising means for saving the adaptive parameters of an adaptive device located within said receiver and calculated by said DSP if said frame check sequence indicates that said received signal is error free.

21. The program as defined in claim 19, further comprising means for using existing parameters of an adaptive device located within said receiver if said frame check sequence indicates that said received signal contains errors.

22. The program as defined in claim 19, wherein said DSL device operates in a multipoint environment.

23. The program as defined in claim 19, wherein said DSL device operates in a half duplex environment.

24. The program as defined in claim 19, wherein said DSL device operates in a full duplex environment.

25. The program as defined in claim 19, wherein said DSL device operates in an asymmetrical duplex environment.

26. The program as defined in claim 19, wherein said means for performing layer two error detection occurs in layer one of the OSI seven layer model.

27. The program as defined in claim 20, wherein said means for saving the adaptive parameters of an adaptive device located within said receiver occurs in layer one of the OSI seven layer model.

ABSTRACT

A DSL device performs a frame check sequence operation in a digital signal processor (DSP), *i.e.*, layer one of the OSI seven layer model, heretofore performed only in layer two of the OSI seven layer model. Performing the layer two framing and calculating the frame check sequence in the DSP allows the DSP to use the layer two error detection results, and optionally, the mean squared error vector, to more accurately determine whether to update adaptive receiver parameters.

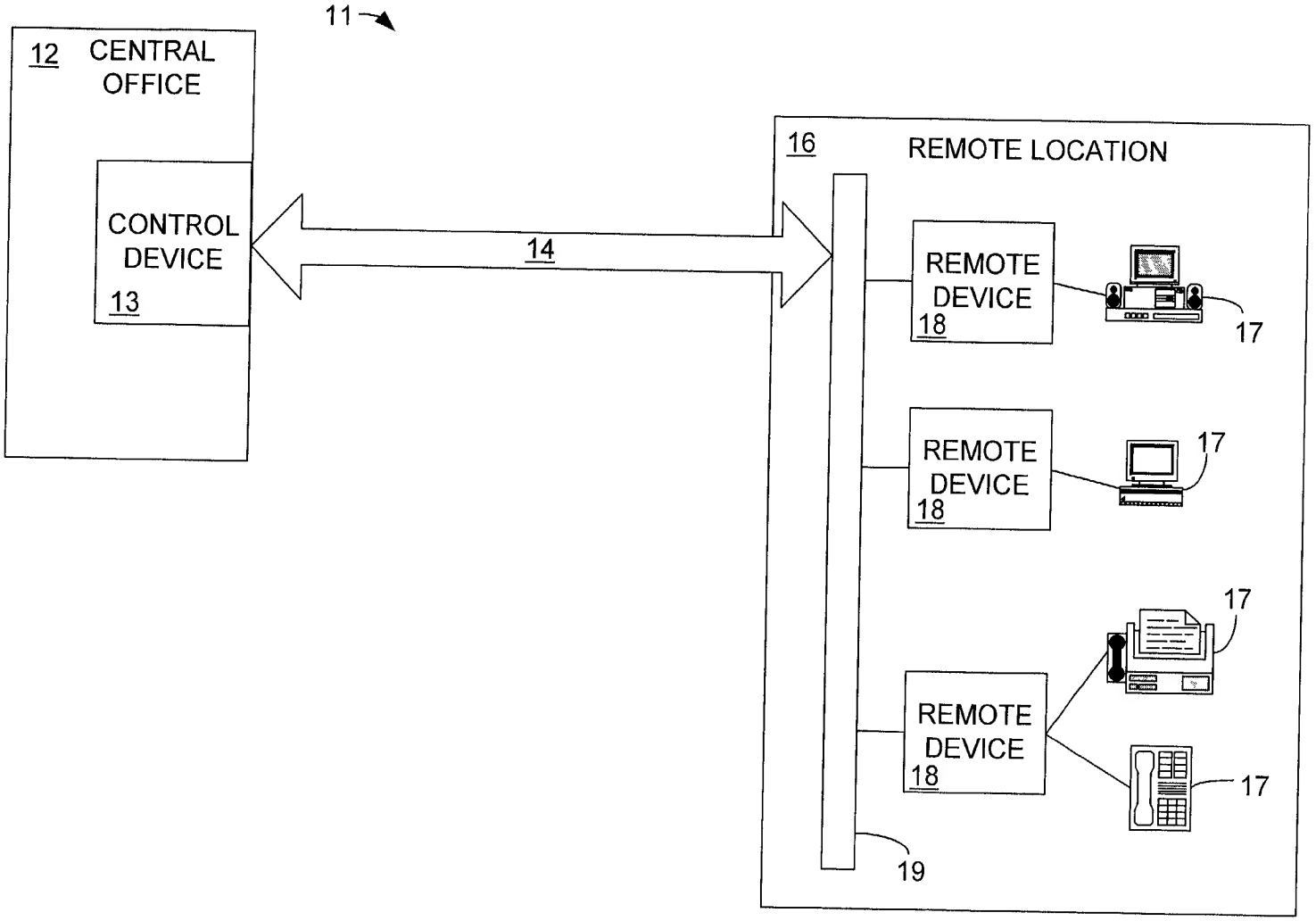

11
12
CENTRAL OFFICE
CONTROL DEVICE
13
14
16
REMOTE LOCATION
REMOTE DEVICE
18
17
REMOTE DEVICE
18
17
REMOTE DEVICE
18
17
17
19

Fig. 1

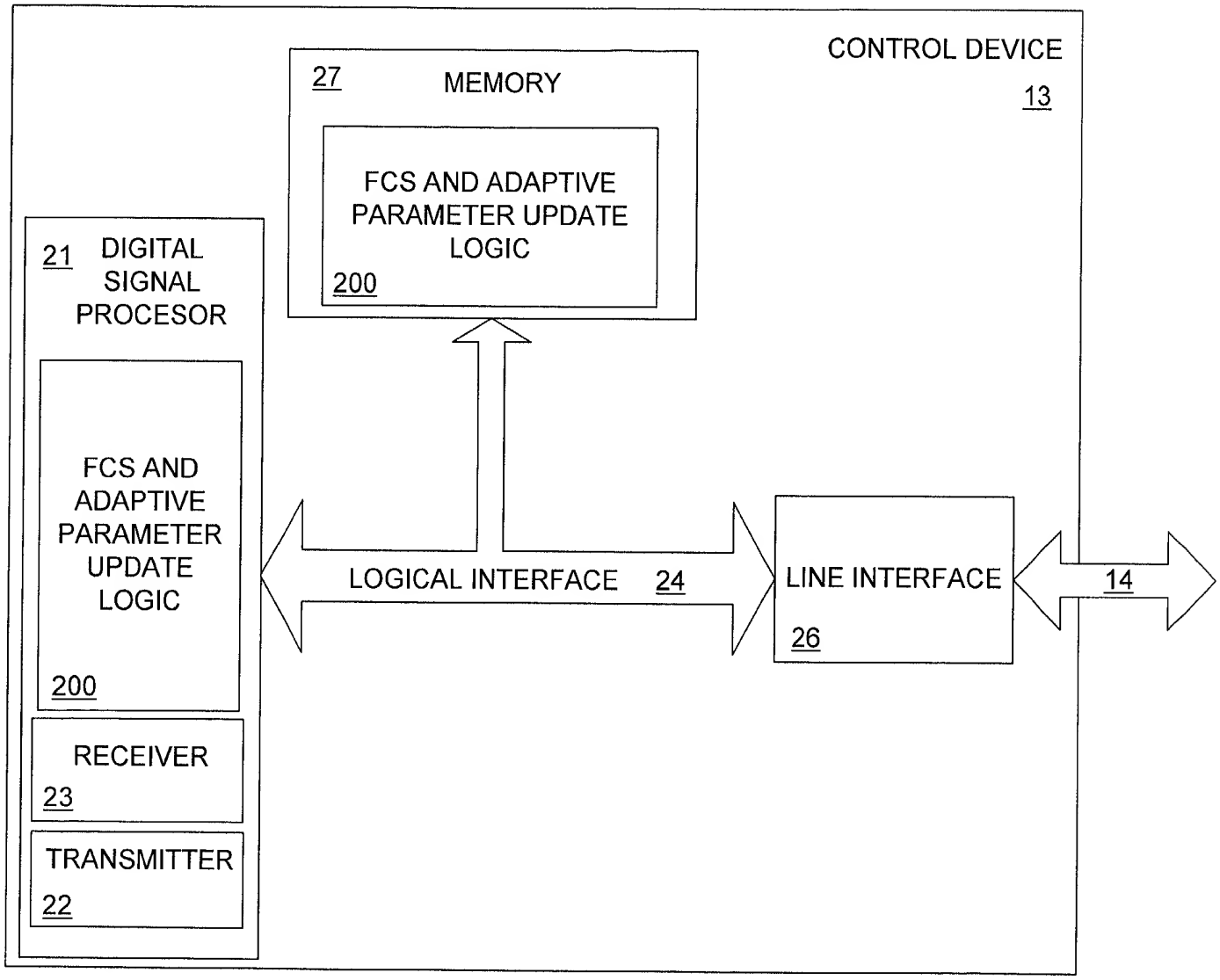

CONTROL DEVICE
13
27
MEMORY
FCS AND ADAPTIVE PARAMETER UPDATE LOGIC
200
21
DIGITAL SIGNAL PROCESOR
FCS AND ADAPTIVE PARAMETER UPDATE LOGIC
200
RECEIVER
23
TRANSMITTER
22
LOGICAL INTERFACE
24
LINE INTERFACE
26
14

Fig. 2

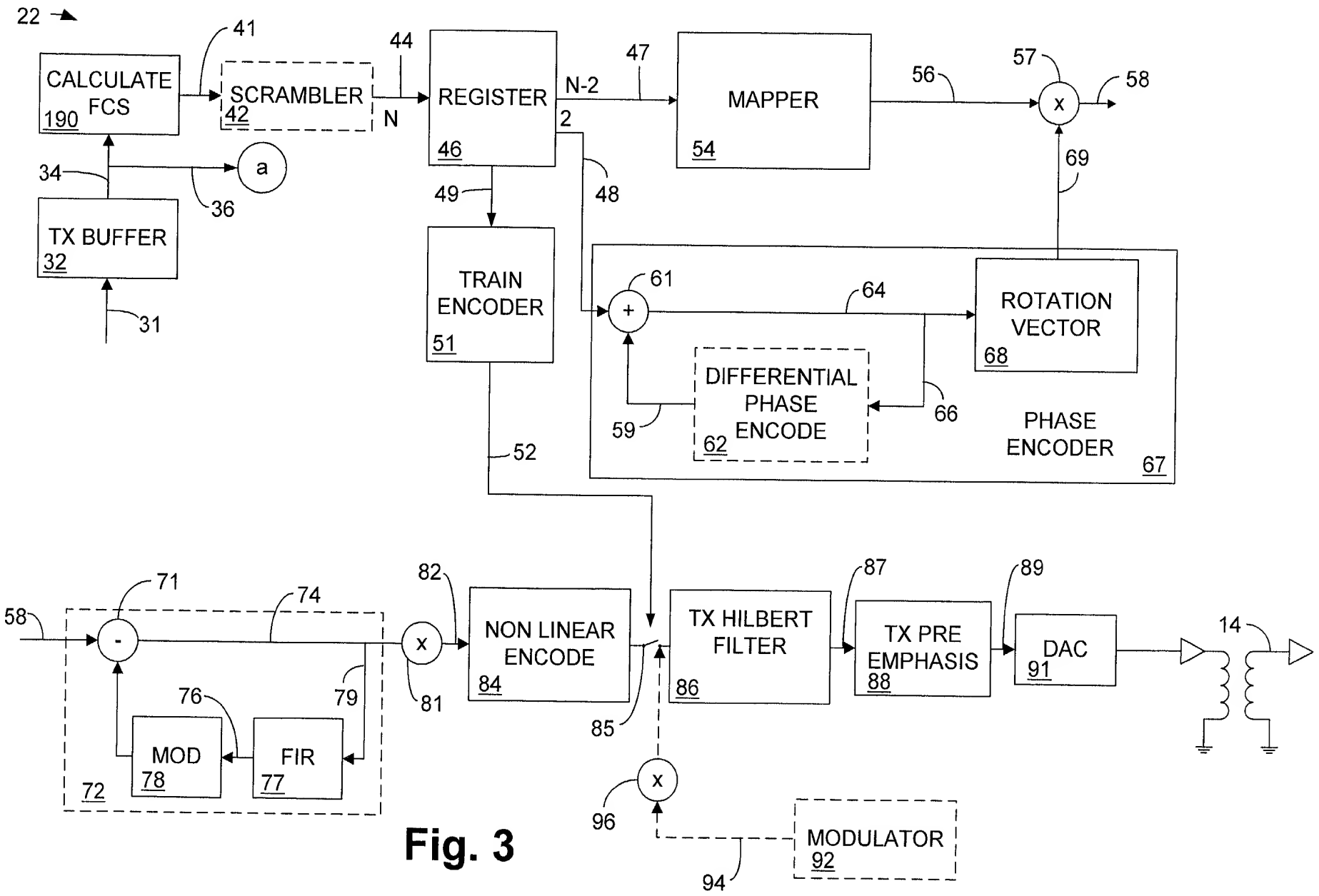
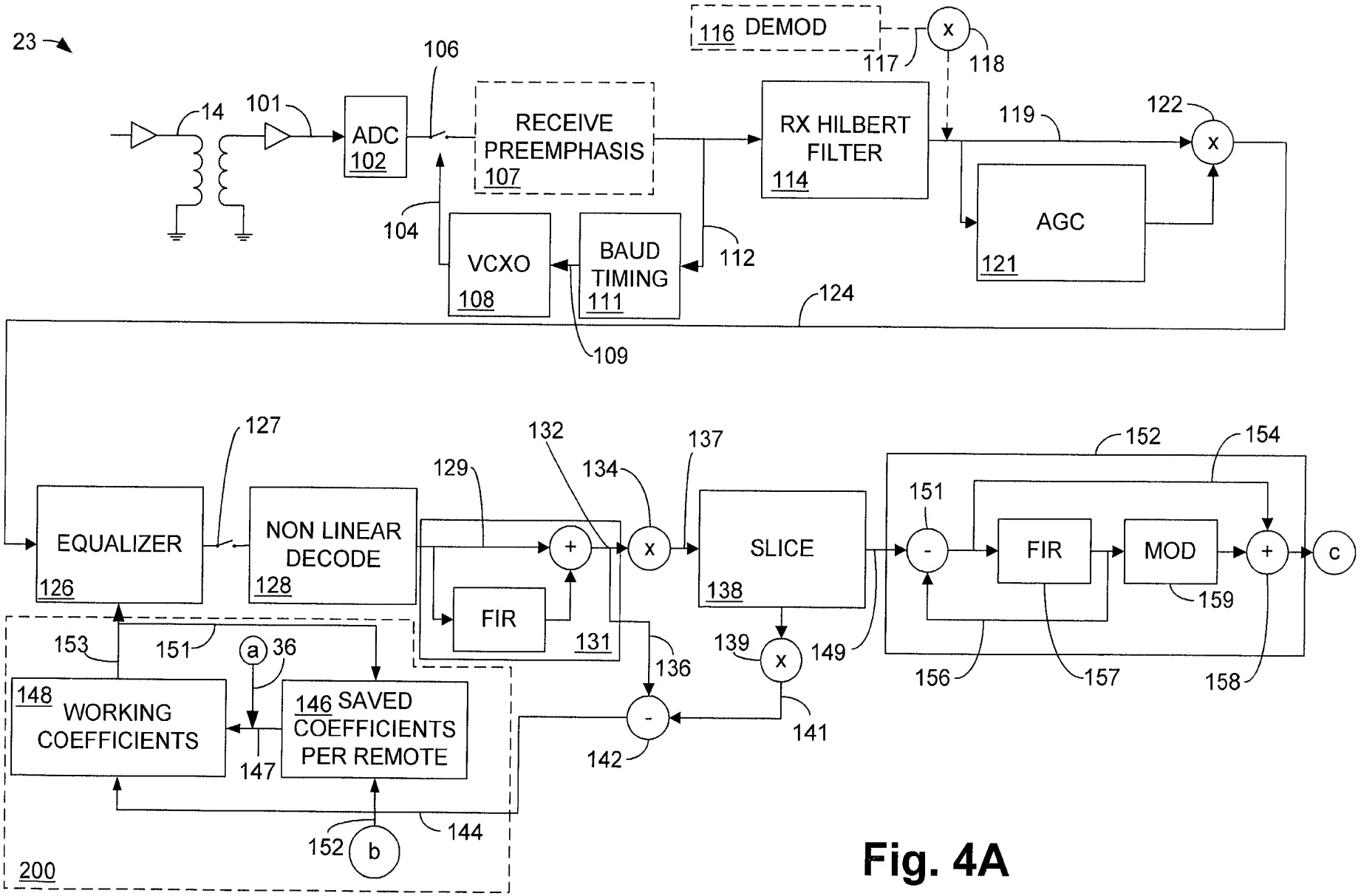


Fig. 3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116 DEMOD
117
118
x
106
14
101
ADC
102
RECEIVE
PREEMPHASIS
107
RX HILBERT
FILTER
114
119
122
x
104
VCXO
108
BAUD
TIMING
111
112
AGC
121
124
109
127
132
129
134
137
152
154
151
EQUALIZER
126
NON LINEAR
DECODE
128
+
x
SLICE
138
-
FIR
MOD
+
c
FIR
131
153
151
a
36
136
139
x
149
148
WORKING
COEFFICIENTS
146 SAVED
COEFFICIENTS
PER REMOTE
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-
141
142
156
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152
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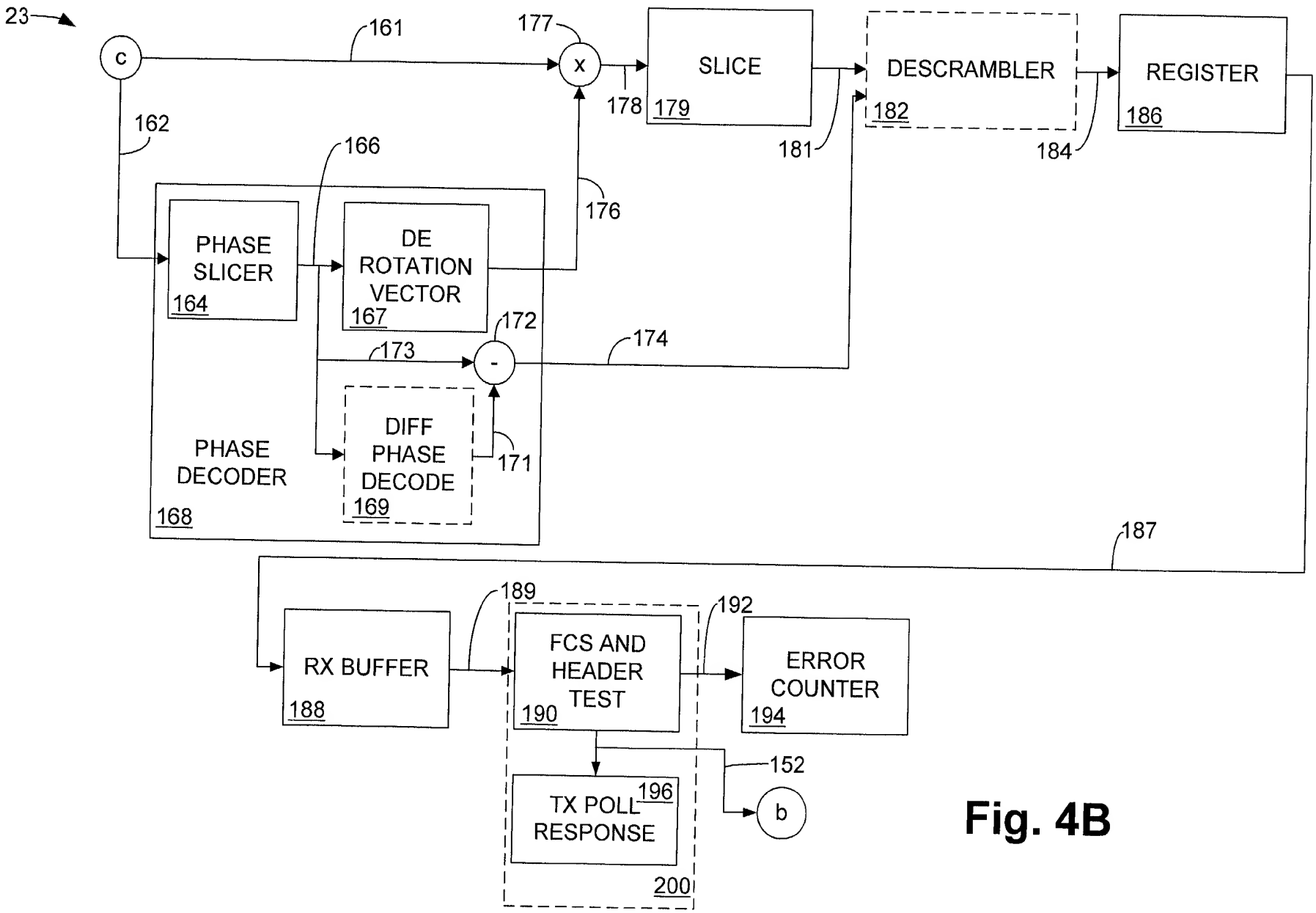
144
200

Fig. 4A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SLICE
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164
DE ROTATION VECTOR
167
172
173
174
-
DIFF PHASE DECODE
169
171
PHASE DECODER
168
187
189
192
RX BUFFER
188
FCS AND HEADER TEST
190
ERROR COUNTER
194
152
196
TX POLL RESPONSE
b
200

Fig. 4B

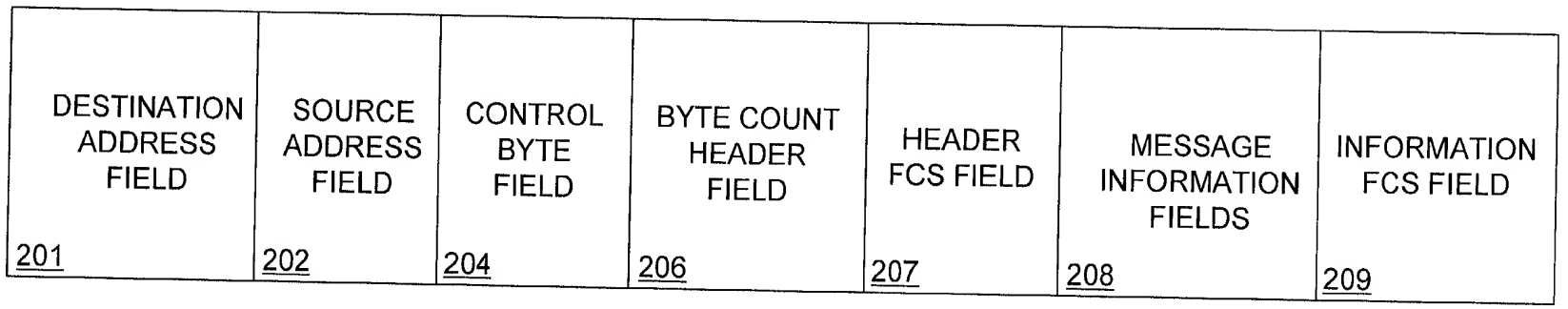

Fig. 5

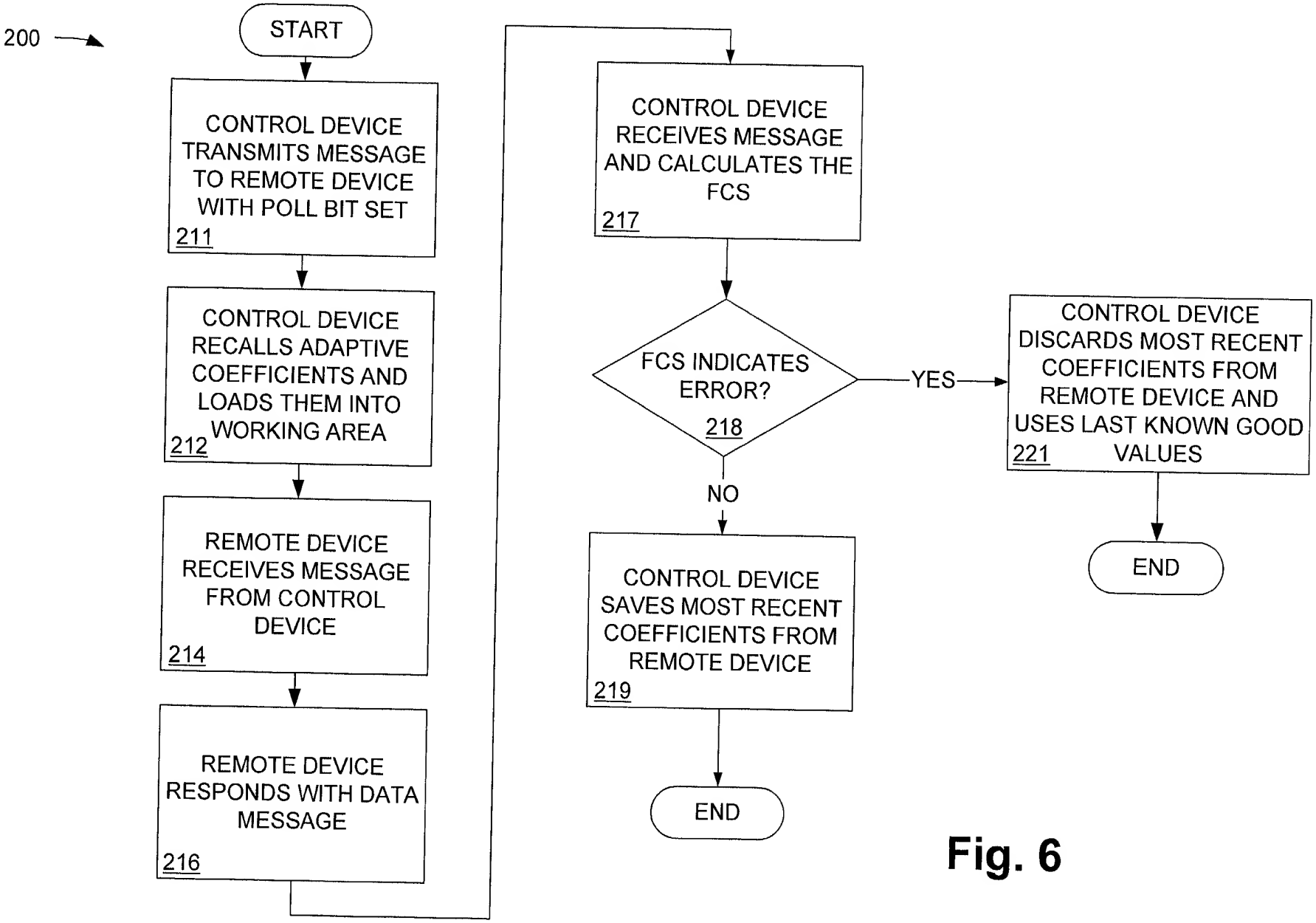
200
START
CONTROL DEVICE TRANSMITS MESSAGE TO REMOTE DEVICE WITH POLL BIT SET
211
CONTROL DEVICE RECALLS ADAPTIVE COEFFICIENTS AND LOADS THEM INTO WORKING AREA
212
REMOTE DEVICE RECEIVES MESSAGE FROM CONTROL DEVICE
214
REMOTE DEVICE RESPONDS WITH DATA MESSAGE
216
CONTROL DEVICE RECEIVES MESSAGE AND CALCULATES THE FCS
217
FCS INDICATES ERROR?
218
YES
CONTROL DEVICE DISCARDS MOST RECENT COEFFICIENTS FROM REMOTE DEVICE AND USES LAST KNOWN GOOD VALUES
221
END
NO
CONTROL DEVICE SAVES MOST RECENT COEFFICIENTS FROM REMOTE DEVICE
219
END

Fig. 6

DECLARATION FOR PATENT APPLICATION

Attorney Docket No: **61606-1240**

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am an original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled **Apparatus And Method To Allow A Frame Check Sequence To Determine The Updating Of Adaptive Receiver Parameters Of A High Speed Communication Device**, the specification of which:

- ☒ is attached hereto.
- ☐ was filed on _____ as Application Serial No. _____.
- ☐ was filed on _____ under U.S. Express Mail No. _____.
- ☐ was described and claimed in PCT International Application No. _____; filed on _____ and as amended Under PCT Article 19 on _____ (if any).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim the benefit under Title 35, United States Code, §119 of any United States provisional patent application, foreign application(s) for patent or inventor's certificate listed below and have also identified below any United States provisional patent application, foreign application for patent or inventor's certificate having a filing date before that of the above-identified application on which priority is claimed: **The Frame Check Sequence Determines Updating A High-Speed Multipoint Modem's Equalizer Coefficients, assigned serial number 60/036,006, and filed March 5, 1997.**

I hereby claim the benefit under Title 35, United States Code, §120 of any United States patent application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I/we acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application: **NOT APPLICABLE.**

I hereby appoint the following attorneys/agents to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: **Jeffrey R. Kuester: Reg. No. 34,367; George M. Thomas: Reg. No. 22,260; James W. Kayden: Reg. No. 31,532; Scott A. Horstemeyer: Reg. No. 34,183; Stephen R. Risley: Reg. No. 35,659; Daniel J. Santos: Reg. No. 40,158; Daniel R. McClure: Reg. No. 38,962; John A. Savio: Reg. No. 36,665; Robert E. Stachler II: Reg. No. 36,934; David P. Kelley: Reg. No. 17,420; Michael J. Tempel: Reg. No. 41,344; Michael J. D'Aurelio: Reg. No. 40,977; David R. Risley: Reg. No. 39,345; Jon E. Holland: Reg. No. 41,077.**

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Atlanta, Georgia 30339-5948

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statement and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Inventor's Signature: _____ Date: Feb 04, 1998

Full Name of First or Sole Inventor: **Joseph Quinn Chapman**
Residence: **9040 Baywood Park Drive, Seminole, Florida 33777** Citizenship: **U.S.A.**
Post Office Address: **9040 Baywood Park Drive, Seminole, Florida 33777**

Inventor's Signature: _____ Date: _____

Full Name of Second Inventor: _____
Residence: _____ Citizenship: _____
Post Office Address: _____

Inventor's Signature: _____ Date: _____

Full Name of Third Inventor: _____
Residence: _____ Citizenship: _____
Post Office Address: _____